REMARKS/ARGUMENTS

Claim Status

Claims 1-52 are pending. Claims 1-14, 17, 20, 21, 28-33, 36, 38-43, and 46 stand rejected. Claims 1-19 stand rejected as being indefinite under 35 U.S.C. § 112. Claims 1, 2, 5, 8, 10, 12, 13, 14, 17, 20, 21, 28-33, 36, 38-43, and 46 stand rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,578,131 to Larson et al. (hereinafter "Larson"). Claim 9 stands rejected under 35 U.S.C. § 103 as being unpatentable over Larson. Claim 11 stands rejected under 35 U.S.C. § 103 as being unpatentable over Larson in view of U.S. Patent No. 6,567,873 to Henriksen (hereinafter "Henriksen").

Claims 15, 16, 18, 19, 22-27, 32-35, 37, 44, 45, and 47-52 stand objected to, but allowable if rewritten appropriately. Applicant appreciates the examiner's indication of allowable subject matter. Applicant maintains the patentability of claims 1-52 and respectfully requests reconsideration and withdrawal of the rejections and objections to claims 1-52.

Claim 1 has been amended. No new matter has been added. The amendment finds support in the application as originally filed at least in Figure 1.

Claim Rejections - 35 U.S.C. § 112

Claims 1-19 stand rejected as being indefinite under 35 U.S.C. § 112, second paragraph, as allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, as amended, recites that the crossbar structure of the multiple processor computer system *connects the plurality of processors to the shared resource.* As such, applicant respectfully submits that claim 1, and claims dependent therefrom including claims 2-12, meet the requirements of 35 U.S.C. § 112, second paragraph.

Claim 13 is directed to a *crossbar structure* (in contrast to a system) for use in a multi-processor computer system to connect a plurality of processors to at least one shared resource. The crossbar structure includes, for each processor, a corresponding storage location *for receiving from the respective processor* a memory address of a lock control structure associated with the shared resource. To acquire a lock, the crossbar structure, *on*

behalf of a processor, performs memory operations on the *lock control structure at the address specified in the corresponding storage location* in order to acquire the lock on behalf of the processor. As such, applicant submits that the claim includes relationships between elements that cooperate with the crossbar structure (*e.g.*, the processor, the lock control structure associated with the shared resource). Therefore, applicant respectfully submits that claim 13, and claims dependent therefrom including claims 14-19, meet the requirements of 35 U.S.C. § 112, second paragraph.

Accordingly, applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 112 rejection of claims 1-19.

Claim Rejections - 35 U.S.C. § 102 and 103

Independent claims 1, 13, 20, 28, and 38 recite features that are not disclosed or suggested by the cited references, either taken alone or in combination, namely as represented by claim 1:

1. (Currently Amended) A multiple processor computer system comprising:
a plurality of processors;
a shared resource;
a main memory in communication with the plurality of processors, at least a portion thereof comprising a control structure for controlling a lock on said shared resource; and
a *crossbar structure* connecting the plurality of processors to the shared resource for controlling access among the processors to the shared resource, the crossbar structure comprising, for each processor, a corresponding storage location, one of the plurality of processors writing to a storage location corresponding to the one processor, an address of the lock control structure associated with said shared resource to acquire the lock thereto, the crossbar structure, on behalf of the one processor, performing memory operations on the lock control structure at the address specified in the corresponding storage location in order to acquire the lock on behalf of the one processor. (emphasis added)

Applicant respectfully submits that Larson does not disclose or suggest a *crossbar structure*. In the application as originally filed, a crossbar structure is defined as "a crossbar having the structure described in detail herein or any other hardware bridge or switch that provides an interface to all of the processors of the system" (application at page 7). Larson, in contrast, discloses *microprocessor* 52 performing spinlocks to access a hash table (Larson at Fig. 5). Because microprocessor 52 performs the spinlocks, bus 56 will have increased

communication traffic. Such a disadvantageous configuration is discussed in the background section of the application at page 2:

> If the processor reads a "locked" status from the lock bit, then that processor does not receive the lock for that resource. If the processor does not receive the lock, the processor continually and repeatedly requests the lock using the test and set instruction described above. This is referred to as the processor "spinning on the lock," because the processor repeatedly requests the lock until it receives the lock. When a *processor* spins on a lock, *it occupies bandwidth on the processor bus*, because each time a processor performs a test and set operation on the memory control structure that includes the lock bit, the processor has to acquire exclusive ownership of that control structure in memory. (emphasis added)

The claims, however, include the feature of the *crossbar structure, on behalf of the one processor*, performing memory operations ... to acquire the lock on behalf of the one processor. In this manner, a processor bus may have improved bandwidth because the crossbar structure acquires the lock for the processor.

Nor does Henriksen cure the deficiencies of Larson. Henriksen discloses a processor 102N connected *directly* to shared I/O 106B *without* a crossbar structure (Henriksen at Figure 1).

Accordingly, applicant submits that the cited references do not disclose or suggest the features of independent claims 1, 13, 20, 28, and 38. Additionally, inasmuch as dependent claims 2-12, 14-19, 21-27, 29-37, and 39-52 (which have also been rejected or objected to) are dependent on claim 1, 13, 20, 28, or 38, these claims are patentable over the cited references, at least by virtue of their dependency. Accordingly, applicant respectfully requests reconsideration and withdrawal of the rejections (and/or objections) of claims 1-52 under 35 U.S.C. § 102 and 103.

Conclusion

For the foregoing reasons, applicants respectfully submit that all of the claims of the present application patentably define over the cited references of record, alone or in combination. Reconsideration of the office action and an early notice of allowance are respectfully requested. In the event that the examiner cannot allow the present application for

any reason, the examiner is encouraged to contact the undersigned attorney, Raymond N. Scott Jr. at (215) 564-8951, to discuss resolution of any remaining issues.

Date: February 5, 2004

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